VLSI Final Exam (Cmpt 421.3 and 814.3)

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This exam consists of ten short questions (approximately) taken from the reading quizzes (worth 5 points each) and one long question regarding the design of a VLSI application (worth 50) points. The long question is open-ended: use it as an opportunity to demonstrate the breadth and depth of your understanding of the fundamental issues of VLSI systems and design. Good luck, and Merry Christmas!

1) [5] Sketch a side view of a CMOS inverter. Label all materials. Label all electrical terminals. Indicate where pn-junctions form when the gate is on.

2) [5] State Moore's law. What are the reasons Moore's law may fail to continue to hold in the next decade or two?

3) [5] Identify three sources of parasitic delay in CMOS circuits.

4) [5] In regard to the consumption of power by CMOS circuits: how does clocking frequency affect power use?, how do transistor width and length affect power use? How do transistor width and length affect circuit speed?

5) [5] Sketch a domino CMOS NOR gate. Briefly explain its operation.

6) [5] In a circuit with some arbitrary combinational logic between the D and Q of a Master-Slave Flip-Flop (MS-FF), where the MS-FF captures a new state during the off period of the clock and outputs its new state after the rising edge of the clock, identify (in a timing diagram of the clock) the relative positions of: the set-up time of the MS-FF, the hold time of the MS-FF, and the combinational delay time.

7) [5] What factors determine the speed of an nMOS PLA?

8) [5] What is a "windmill"?. What problems do they create for the definition of routing channels and the wiring of a placed design.

9) [5] Identify three important characteristics which distinguish VLSI chip packages?

10) [5] What is the difference between "timing analysis" and "timing simulation"? When is each timing method useful?

11) [50] Suppose you have been assigned the job of designing, implementing, and testing a special-purpose VLSI memory array. The memory is to consist of 256 64-bit words; it is to be dual-ported, allowing one independent write and one independent read per cycle (possibly to/from the same word). The memory is to be designed to run as fast as reasonable in a 0.5μm twin-tub CMOS with four layers of metal, but no enhanced polysilicon wires. While speed is to be emphasized, area and power cannot be ignored.

Your assignment, for this question, is to:

a) describe how the design, implementation, and testing processes would be carried out, and

b) identify key issues (regarding the memory cell, the buses, the clock, and the address decoders) and either make design choices on these issues (explaining the motivation for each choice), or select several possible approaches and explain how the choices between the options would be made.